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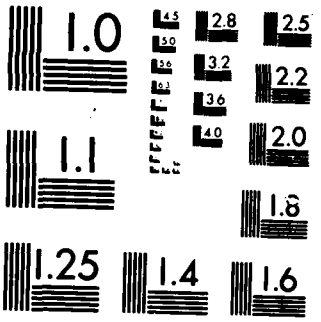

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AFGL-TR-85-0112

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MODEL 2480 TIMER

by

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"This technical report has been reviewed and is approved for publication"

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FOR THE COMMANDER

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Presented is a summary of the design and development of a sounding rocket payload timer, under Contract F19628-81-C-0029. The specific unit described in this report is the Model 2480 which includes logic relays as well as the digital timing circuit. Included are operating principles, component identification, configuration, available options and the luanch vehicles for which the timer has been qualified.

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TABLE OF CONTENTS

ILLUSTRATIONS

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1. INTRODUCTION

The Model 2480 timer is a digital memory device whose stored program is read out at a specific, precisely timed rate. It was designed to provide a pre-programmed flight sequence for sounding rocket payload systems. Contract No. F19628-81-C-0029 provides engineering support for a wide variety of scientific experiment packages and launch vehicles that require timing. The basic timer configuration described in this report has been adapted to several payloads and performed functions such as: power turn on; calibration pulses to experiments; motor drive mechanism control; initiation of pyrotechnic eject mechanisms; and timing to other payload modules including attitude control system and supplemental experiment packages.

Features include redundancy capability, low power consumption, selectable clock rates and timing intervals, flexible output relay configuration, and total running times of up to 136 minutes.

2. DESIGN REQUIREMENTS

Reliability and flexibility were the primary design criteria. Initially the requirements of previous payloads were reviewed and attempts were made to optimize the timer/relay interfaces. Timing requirements from several programs were also considered in order to select timing increments, total flight times and the total number of functions required.

Efforts were also directed to minimizing power and size of the timer. The Model 2480 draws less than 50 milliamperes from a typical 28 volt payload battery. Adaptability to a nine-inch diameter

payload structure was defined as the mechanical constraint. Environmental specifications for the Nike-Tomahawk vehicle served as the minimum qualification design level for the timer package.

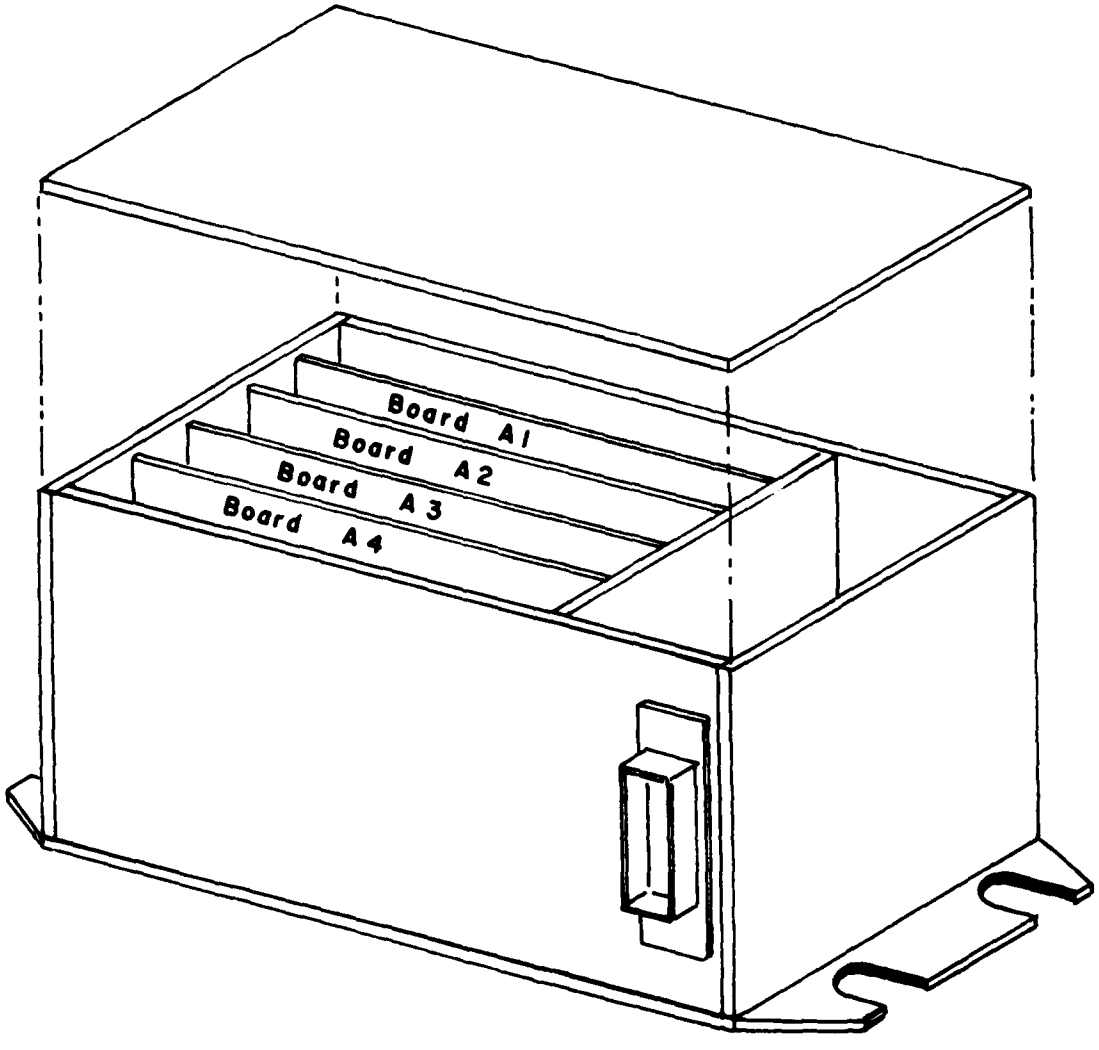
A 2716 EPROM (Erasable Programmable Read Only Memory) with a capacity of up to 16K-bits was selected as the memory element. A 24-pin socket interfaces the EPROM, which must be physically removed from the timer for programming.

3. CONFIGURATION

Previous digital timer/logic systems consisted of a timing module packaged on wire-wrap panels, and external logic relays to interface with the experiments and support systems. Investigations led to an integral timer/logic unit with five (5) printed circuit boards. The overall timer package is 6.5-inches X 3.5-inches X 3.25-inches and weighs approximately 2.6 lbs. Individual screw fastened plates allow access to various parts of the timer without complete disassembly. As indicated in Figure 1 the base plate (7.25-inches X 3.56-inches) accommodates deck mounting with four #10 screws. Two 50-pin input/output connectors provide the payload electrical interface.

Timer components are mounted on four (4) printed circuit boards (A1 through A4) which plug into a "mother" printed circuit board (A5). The A5 board routes signals and power between the four component boards and to the payload interface connectors. The component boards are defined as follows:

A1 - Clock Board: Includes the crystal oscillator, counters and timer control relays (start and enable).



MODEL 2480 TIMER

FIGURE 1

A2 - EPROM Board: Includes the 2716 EPROM, latches, addressing circuits, and diagnostic circuits.

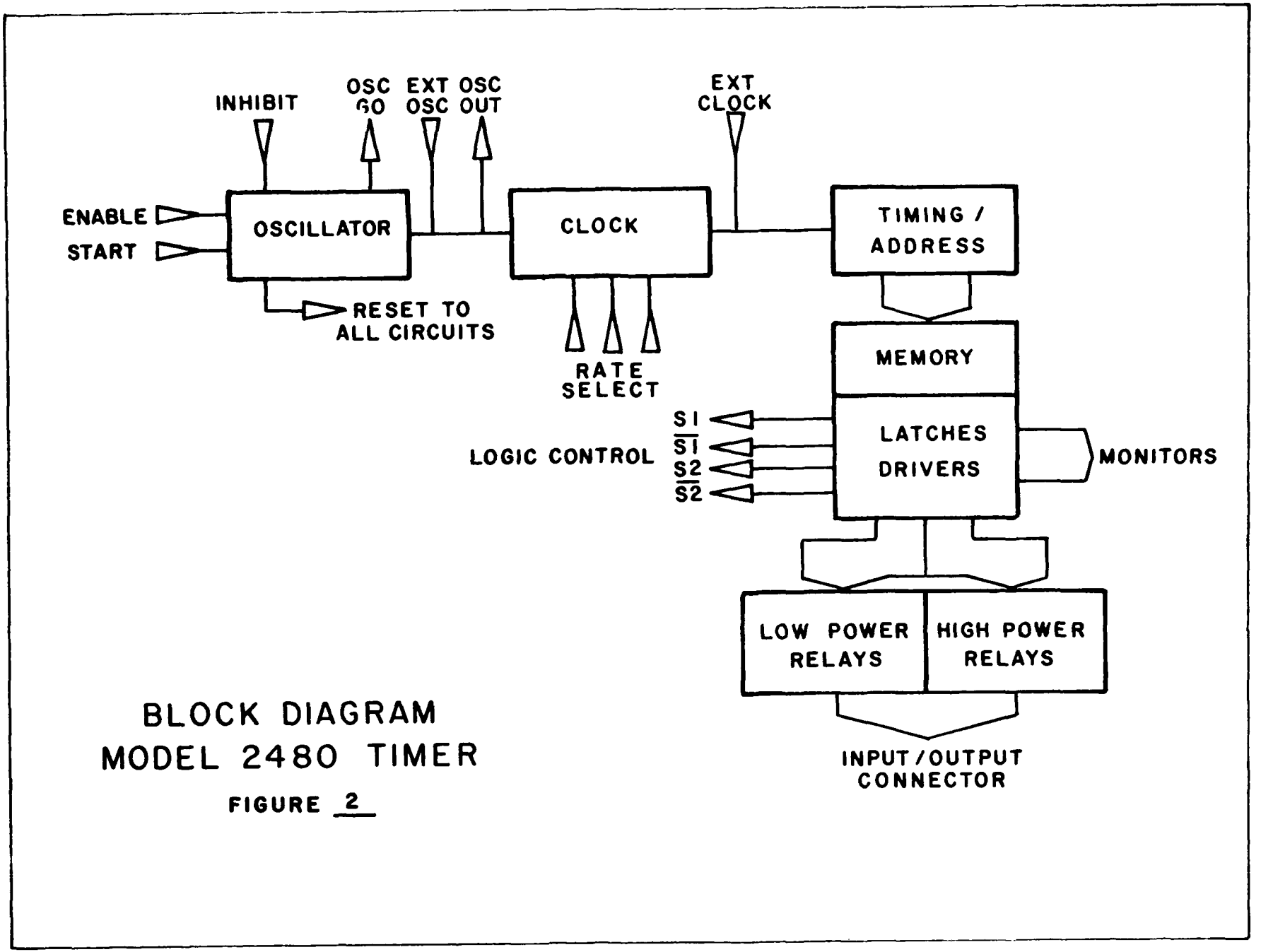
A3 - Relay Board: Has provisions for ten SPDT relays. Relay configuration is selected for the specific payload application.

A4 - Power Relay Board: Has provisions for eight DPDT relays. Relay configuration, including latching or non-latching option, is selected for the specific payload application.

A master drawing was generated for use when adapting a timer system to a specific application. Standard control circuits and input/output interfaces are included, as well as all available relay and wiring options. Initially a copy of this drawing is used to define the timer/payload interface and ultimately for assembly and wiring of the timer.

4. OPERATION

Figure 2 illustrates the six (6) basic functions of a single timer. A stable, high frequency OSCILLATOR is used as a time base. Elapsed time is measured in pre-programmed increments generated by the CLOCK circuit. These increments are then used in TIMING/ADDRESS circuits to access the flight program at each increment transition. Required flight data is programmed into erasable programmable read only memory (EPROM), external to the timer. Data stored in MEMORY is held by the LATCHES until the next time increment and conditioned by the DRIVERS to operate the payload control relays. The LOW POWER



BLOCK DIAGRAM
MODEL 2480 TIMER

FIGURE 2

RELAYS can switch up to one ampere at 28 volts. These single pole double throw (SPDT) relays are non-latching, but may be held on for any period in the flight program. The double pole double throw (DPDT) HIGH POWER RELAYS are used for power transfer and pyrotechnic activation and may be either latching or non-latching. The following sections detail timer operation.

4.1 Clock Board (A1)

A precision (32.768KHz) crystal clock oscillator is used as a timing source. A binary divider chain reduces the oscillator square-wave by a factor of 2 in each of eighteen stages. The last eight stages of this chain are connected to an eight position electronic "switch" called the rate selector. The position of this "switch" is determined by the binary code present on the three rate select lines, and one of the following clock rates becomes the fundamental time increment: 1/16th. sec., 1/8th. sec., 1/4 sec., 1/2 sec., 1 sec., 2 sec., 4 sec., or 8 sec. The rate select lines may be "programmed" in any of three ways: logic level jumpers in an area provided on printed circuit board; under control of the stored flight program through the logic control lines; or under external control (command receiver, etc.). These options allow the user to control not only the total operating time of the unit, but also the minimum duration of each relay closure.

The selected clock rate signal is then used to increment an address generator which is in turn connected to the memory element. In order to reduce the number of components, a scheme was developed to effectively double the workload of the memory section. This entails

using paired addresses in the memory, accessed every clock cycle to operate sixteen relay control lines simultaneously from an eight bit output. Power consumption in the timer is reduced by forcing the memory device into a standby mode until the beginning of a clock cycle. Precision monostable multivibrators are responsible for the timing logic needed in the address, memory and latch circuits. A binary divider chain again halves the clock signal eleven times; but this time all eleven stages output simultaneously and are used as address lines to the EPROM on board A2.

A simplified schematic of the A1 board is depicted in Figure 3. Component identification is as follows:

Y1 - QT4C 32.768KHz Crystal Clock Oscillator

U1 - 4009 Hex Inverting/Buffer

U2 - 4071 Quad. Two Input "or" Gate

U3 - 4071 Quad. Two Input "or" Gate

U4 - 4081 Quad. Two Input "and" Gate

U5 - 4040 12-Bit Binary Counter

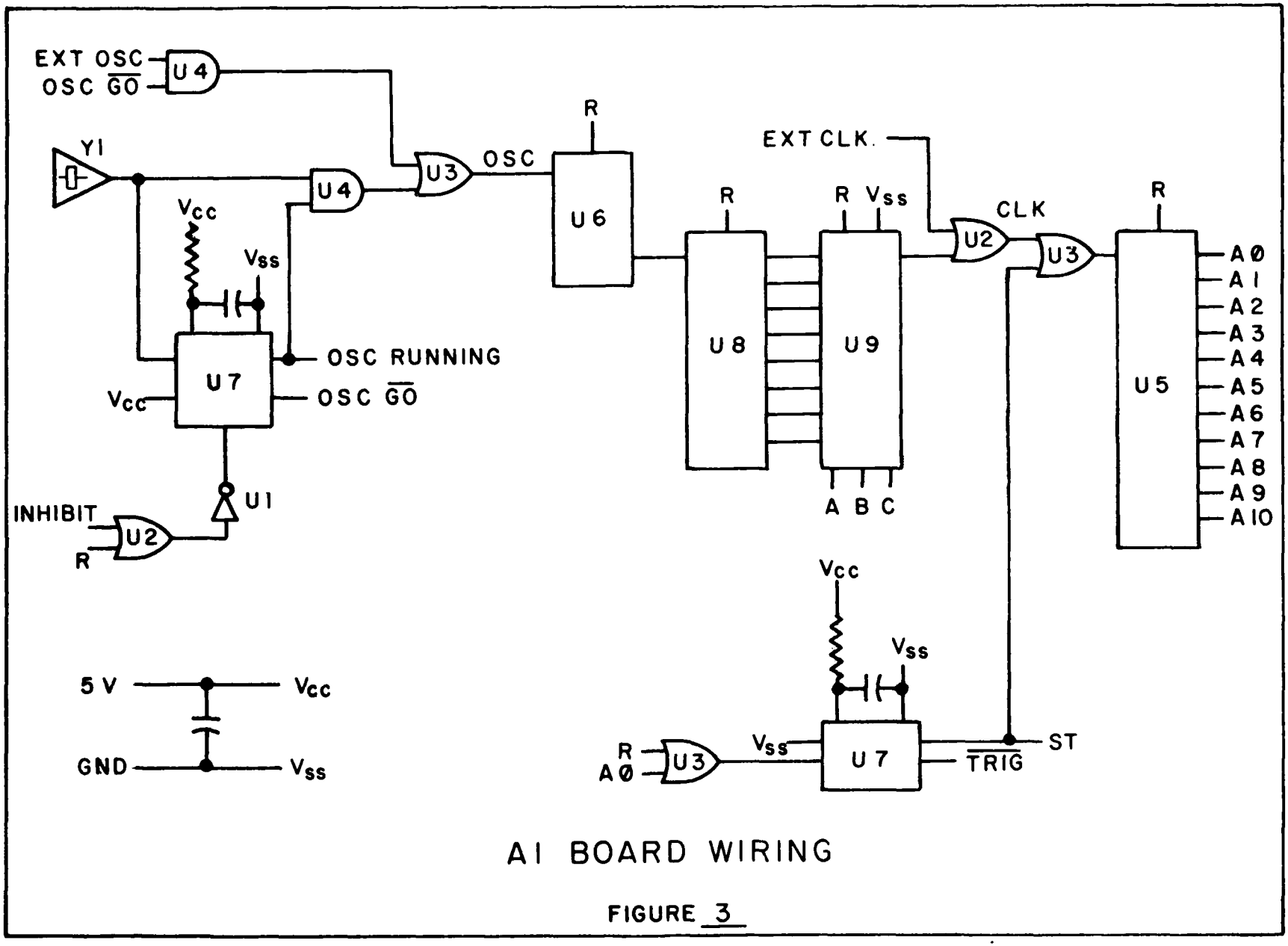
U6 - 4040 12-Bit Binary Counter

U7 - 4528 Dual Monostable Multivibrator

U8 - 4404 8 Stage Binary Counter

U9 - 4512 8 Channel Data Selector

Control relays for timer operation are also included on the A1 board. A latching relay is used for timer enable and a non-latching relay starts the timing sequence. The relays hold a master reset signal on all timer circuits until the latching relay is remotely switched to the enable position and power is removed from the start



AI BOARD WIRING

FIGURE 3

relay coil. Once enabled the timers can be started either at T-0 by umbilical pullout or at a predetermined, pre-launch time from the blockhouse control console. The latter is preferred since timer operation can be confirmed prior to launch. Relay status monitors are also available at the timer interface.

4.2 EPROM Board (A2)

The eleven bit address from the A1 board allows the use of a memory device with a capacity of up to 16K-bits. As noted previously the 2716 EPROM was selected and must be removed from the timer and programmed on a remote programmer. It was possible to design the timer with the capability of programming the EPROM in place; however, the removable EPROM concept was deemed more flexible and easier to troubleshoot or replace.

Eight-bits of data are written into and read out of the EPROM at each address, each bit representing a relay control line. As indicated in Figure 4, latches and relay drivers are also included on the A2 board. There are two 8 bit latches whose inputs are connected in parallel to the EPROM output. Timing logic enables one latch or the other at the beginning of alternate addresses. The latches accept new data only when enabled, but output constantly until they receive a master reset. Therefore, all 16 bits appear at the relay drivers even when the EPROM is standing by. Two of these 16 bits from the latches are also used as the logic control lines. These are available in inverted and non-inverted form (S1, $\overline{S1}$, S2, $\overline{S2}$).

High gain transistor arrays serve as relay drivers; ground is applied to the relay control line (also referred to as data lines)

when a driver's input is high. In addition to relay control, five monitor signals are processed by these transistor arrays; their switched ground outputs are intended as GSE and/or telemetry status monitors. The functions are listed as U3 outputs on Figure 4. Components on the A2 board are:

U1 - 2003 Relay Driver

U2 - 2003 Relay Driver

U3 - 2003 Relay Driver

U4 - 4528 Dual Monostable Multivibrator

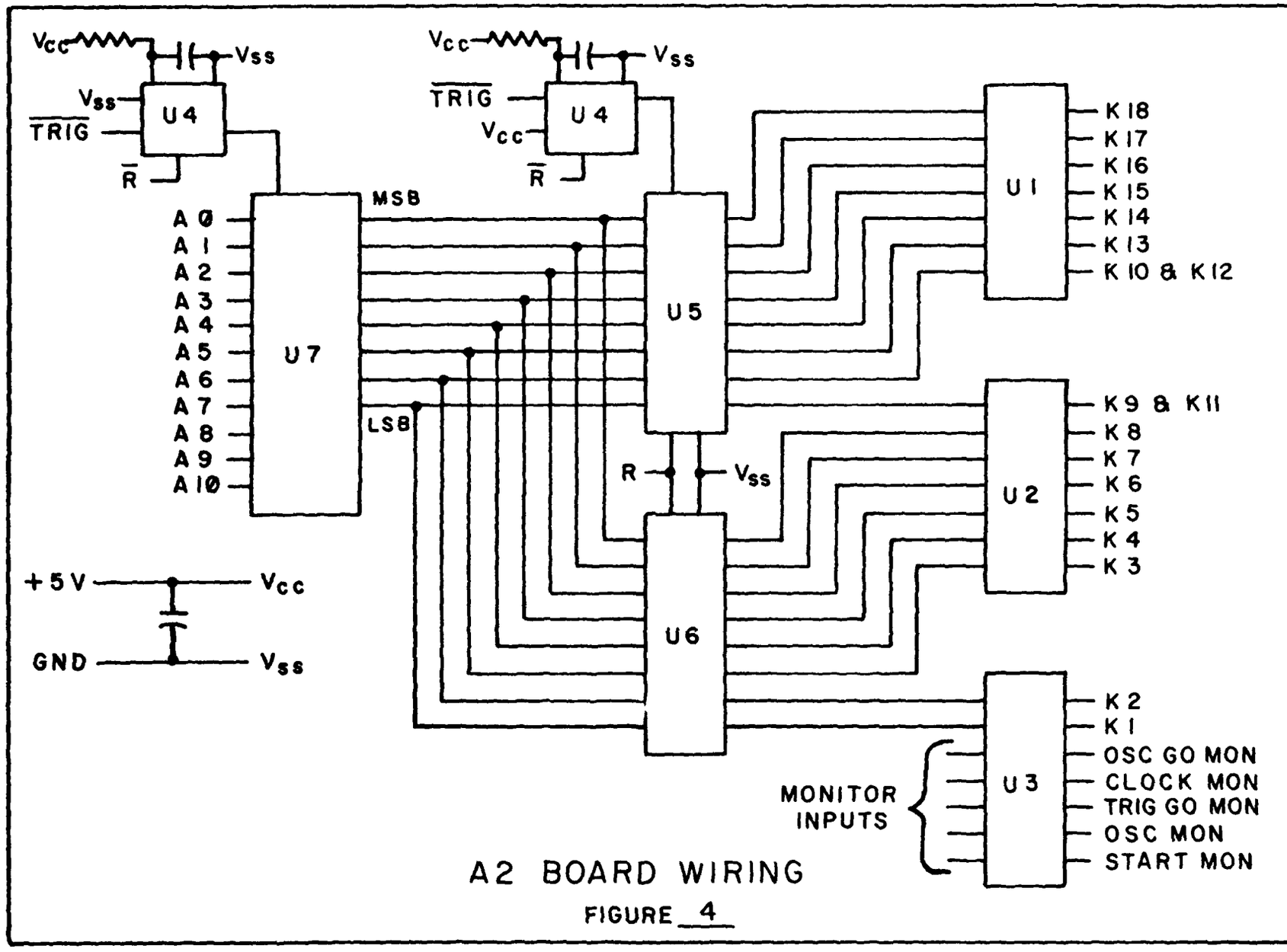
U5 - 4508 Dual 4-Bit Latch

U6 - 4508 Dual 4-Bit Latch

U7 - 2716 16K(2K x 8) UV Erasable Prom

4.3 Low Power Relay Board (A3)

The A3 printed circuit board has provisions for ten SPST (single-pole-single-throw), TO-5 type, non-latching relays labeled K1 through K10. The positive side of all relay coils are wired to a separate +28VDC line; the negative sides of the K1 through K10 coils are connected to data lines 1 through 10 respectively. All K1 to K10 contacts (Normally Closed, Common, Normally Open) are available on the mother board and any combination of these can be brought out to the input/output connectors. The N.C. (Normally Closed) and N.O. (Normally Open) contacts are also available for connection to two independent power busses on the low power board itself. This allows simplified power connection in cases where these relays are switching from common power sources.



A2 BOARD WIRING

FIGURE 4

Although the first 10 data lines are connected to the coils of K1 through K10 respectively, four of these are shared lines: data line 1 is shared between K1 and logic control line S2; data line 2 between K2 and S1; data line 9 is shared between K9 and K11 on the high power board; and data line 10 between K10 and K12. This gives the user the option of any combination of logic control/relay or, low power/high power relay. For instance, it may be desirable to utilize K2 in conjunction with the S1 signal for simultaneous logic and power control. Once the payload interface is designed, only the relays required for that specific application are wired to the A3 board.

4.4 High Power Relay Board (A4)

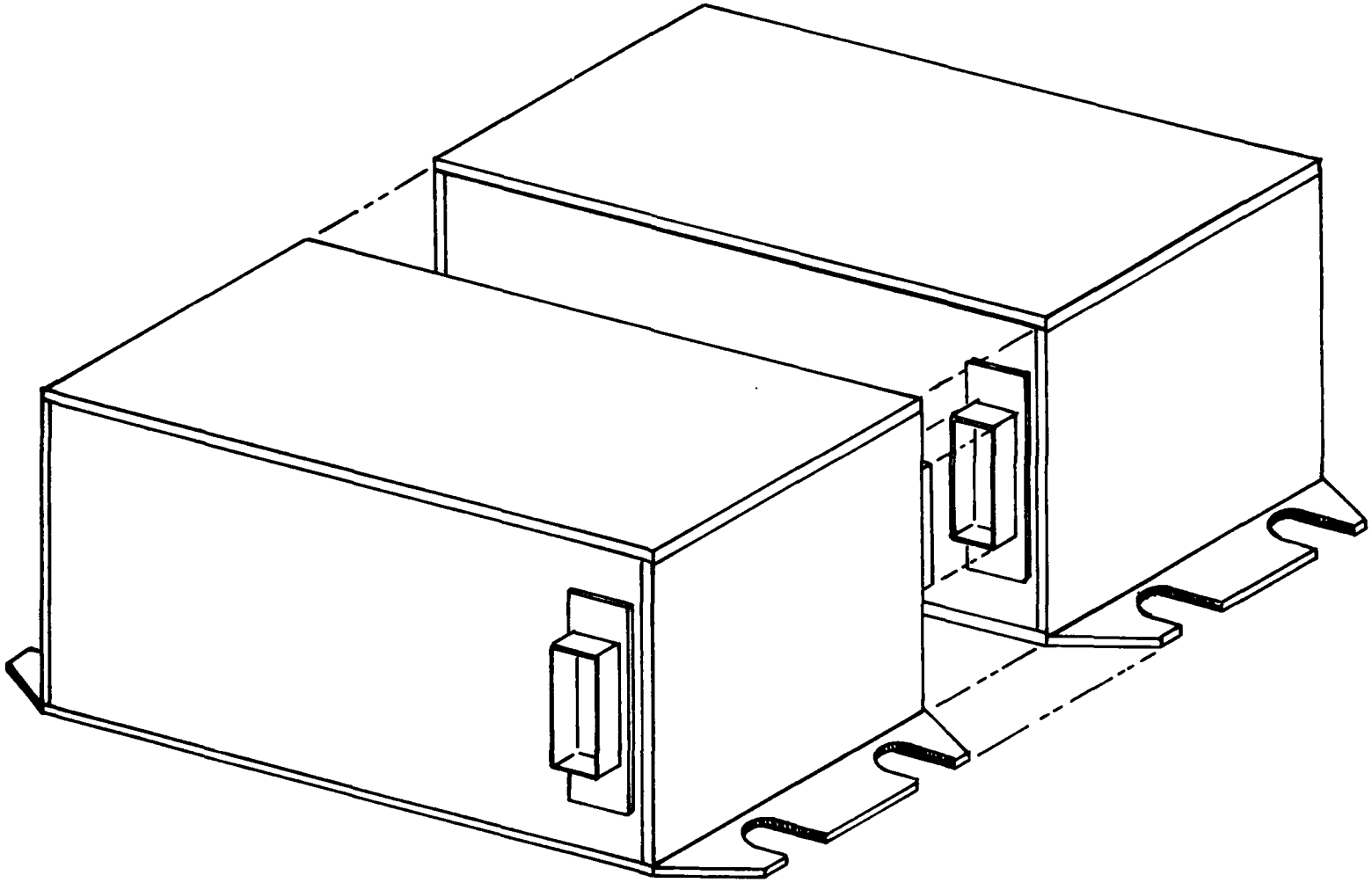
Relays K11 through K18 are half crystal can size DPDT relays whose contacts are rated a 2 amps DC resistive. Either latching or non-latching versions may be selected in all eight positions on the A4 board. Connected to Data Lines 9 through 16 respectively, these relays were included for use in power transfer functions (ON/OFF, INT/EXT), pyrotechnic device activation, or in cases where a latching relay is needed. When the latching version is used, one coil (designated coil A) is connected to a data line, the other coil "reset" (coil B), is made available on the mother board and is also ground seeking. As is the case with the A3 board, bus structures are employed on this board; the assumption being that most high current applications draw power from a common and/or isolated source. This is especially true in the case of pyrotechnics (squibs), where

a short circuit must be held on the bridgewire until activation. Unlike the low power board, the busses here are hard-wired, not optional. Two versions of the A4 board have been used. One has six of the eight relays bussed for pyrotechnic applications and two relays (K11 & K12) wired to the input/output connector. The second type provides for four pyrotechnic and four direct wired relays. During design the appropriate board is selected and only the required relays are wired to the board.

5. REDUNDANCY

Previous sections of this report have described a single timer package capable of providing a maximum of 16 functions. A second timer could of course be added to a payload to increase capacity and/or to provide redundancy. Mechanical design of the package considered this application. When two timers are located side-by-side the 50-pin interface connectors are aligned for direct mating, as indicated in Figure 5. In this configuration the outboard connectors on each timer interface with the payload wiring harness and the mated inboard connectors provide the redundancy interconnections. If side-by-side packaging is not feasible, redundancy can be attained with an interconnecting cable between the inboard connectors.

In order to increase reliability and avoid phasing problems when timers are connected in the redundant mode, it is possible to have both timers derive their clock signals from the same "prime" oscillator. This requires logic circuits in both timers to suppress the



MODEL 2480 REDUNDANT TIMER

FIGURE 5

"back-up" oscillator signal while constantly testing the prime. If the logic detects a failure of the prime oscillator it automatically suppresses it and connects the back-up oscillator to both clock generators. This option has been used in all timers fabricated to date.

6. SUMMARY

A prototype redundant timer system was initially qualified to vibration, shock and thermal environmental specifications of the Nike-Tomahawk vehicle. Subsequently, redundant timers have successfully completed testing programs and were flown on payloads utilizing the following launch vehicles: Nike-Tomahawk, Paiute-Tomahawk, Black Brant VC, Sergeant, and Taurus-Orion.

Timer interfaces proved compatible with the variety of payload requirement and flight profiles above. Currently they are being evaluated for a Minuteman I launch requiring a total flight time in excess of 30 minutes.

APPENDIX A

Related Documents and Contracts

The following internal reports and drawings include detailed information on the Model 2480 Timer:

NU180-5	Timer Assembly Tech. Data
EC-2460	Schematic - A1 Board
EC-2464	Schematic - A2 Board
EC-2468	Schematic - A3 Board
EC-2472	Schematic - A4 Board
C-2481	PC Board Outline - A1 through A4
C-2482	PC Board Outline - A5
D-2998	Assembly - Model 2480 Timer

Previous Contracts:

F19628-67-C-0223	1 April 1967 to 28 February 1970
F19628-70-C-0194	1 March 1970 to 28 February 1973
F19628-73-C-0152	1 March 1973 to 31 May 1976
F19628-76-C-0152	1 May 1976 to 30 April 1981
F19628-81-C-0029	15 February 1981 to present

APPENDIX B

Personnel

The following members of the Electronics Research Laboratory staff contributed to the work reported.

Lawrence J. O'Connor,	Principal Investigator
Richard L. Morin,	Research Associate, Engineer
Robert D. Anderson,	Mechanical Designer
Roger C. Eng,	Mechanical Designer
Charles B. Sweeney,	Electronic Technician
Frederick J. Tracy,	Electronic Technician

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